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Dual Channel Decimating Receiver

12/97 Preliminary AD6620

FEATURES

High Input Sample Rate
- 65 MSPS Single Channel Real
- 32.5 MSPS Dual Channel Real
- 32.5 MSPS Single Channel Complex

NCO Frequency Translation
- Worst Spur better than -100 dBc
- Tuning Resolution better than 0.02 Hz

2ND Order Cascaded Integrator Comb FIR Filter
- Linear Phase, Fixed Coefficients
- Programmable Decimation Rates: 1, 2, 3... 16

5TH Order Cascaded Integrator Comb FIR Filter
- Linear Phase, Fixed Coefficients
- Programmable Decimation Rates: 1, 2, 3... 32

Programmable Decimating RAM Coefficient FIR Filter
- Up to 130 Million Taps per Second
- 256 20-bit Programmable Coefficients
- Programmable Decimation Rates: 1, 2, 3... 32

Bi-directional Synchronization Circuitry
- Phase Aligns NCOs
- Synchronizes Data Output Clocks

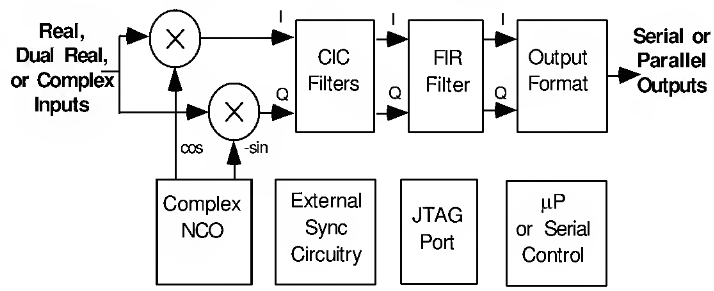
Serial or Parallel Baseband Outputs
- Pin selectable Serial or Parallel
- Serial works with SHARC, AD21XX, most other DSPs
- 16-bit Parallel Port, interleaved I and Q outputs

Two Separate Control and Configuration Ports
- Generic µP Port, Serial Port

3.3 Volt Optimized Process
- Low Power, High Speed CMOS

JTAG Boundary Scan

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD6620 is a digital receiver with four cascaded signal-processing elements: a frequency translator, two fixed-coefficient decimating filters, and a programmable coefficient decimating filter. All inputs are 3.3volt LVCMOS compatible. All outputs are LVCMOS and 5 volt TTL compatible.

As ADCs achieve higher sampling rates and dynamic range, it becomes increasingly attractive to accomplish the final IF stage of a receiver in the digital domain. Digital IF Processing is less expensive, easier to manufacture, more accurate, and more flexible than a comparable highly selective analog stage.

The AD6620 Dual Channel Decimating Receiver is designed to bridge the gap between high speed ADCs and General Purpose DSPs. The high resolution NCO allows a single carrier to be selected from a high speed data stream. High dynamic range decimation filters with a wide range of decimation rates allow both narrowband and wideband carriers to be extracted. The RAM-based architecture allows easy reconfiguration for multi-mode applications.

The decimating filters remove unwanted signals and noise from the channel of interest. When the channel of interest occupies less bandwidth than the input signal, this rejection of out-of-band noise is called "processing gain". By using large decimation factors, this "processing gain" can improve the SNR of an 11-bit ADC by 36dB or more. In addition, the programmable RAM Coefficient filter allows anti-aliasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter.

The input port accepts a 16-bit Mantissa, a 3-bit Exponent, and an A/B Select pin. These allow direct interfacing with the AD6600, AD6640, AD9042 and most other high speed ADCs. Three input modes are provided: Single Channel Real, Single Channel Complex, and Dual Channel Real.

When paired with an interleaved sampler such as the AD6600, the AD6620 can process two data streams in the Dual Channel Real input mode. Each channel is processed with coherent frequency translation and output sample clocks. In addition, external synchronization pins are provided to facilitate coherent frequency translation and output sample clocks among several AD6620s. These features can ease the design of systems with diversity antennas or antenna arrays.

Units are packaged in an 80-pin PQFP (plastic quad flat pack) and specified to operate over the industrial temperature range (-40°C to +85°C).

This information applies to a product currently under development. Characteristics and specifications are subject to change without notice. Consult factory for up-to-date preliminary datasheet.

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AD6620 Preliminary Datasheet Outline

FEATURES
PRODUCT DESCRIPTION
ARCHITECTURE
SPECIFICATIONS
INPUT DATA PORT
FREQUENCY TRANSLATOR
2nd ORDER CASCADED INTEGRATOR COMB FILTER
5th ORDER CASCADED INTEGRATOR COMB FILTER
RAM COEFFICIENT FILTER
PARALLEL OUTPUT DATA PORT
CONTROL REGISTERS AND ON-CHIP RAM
MICROPROCESSOR PORT
SERIAL PORT
PIN DESCRIPTIONS
PIN DESIGNATIONS
APPLICATIONS
PACKAGE OUTLINE

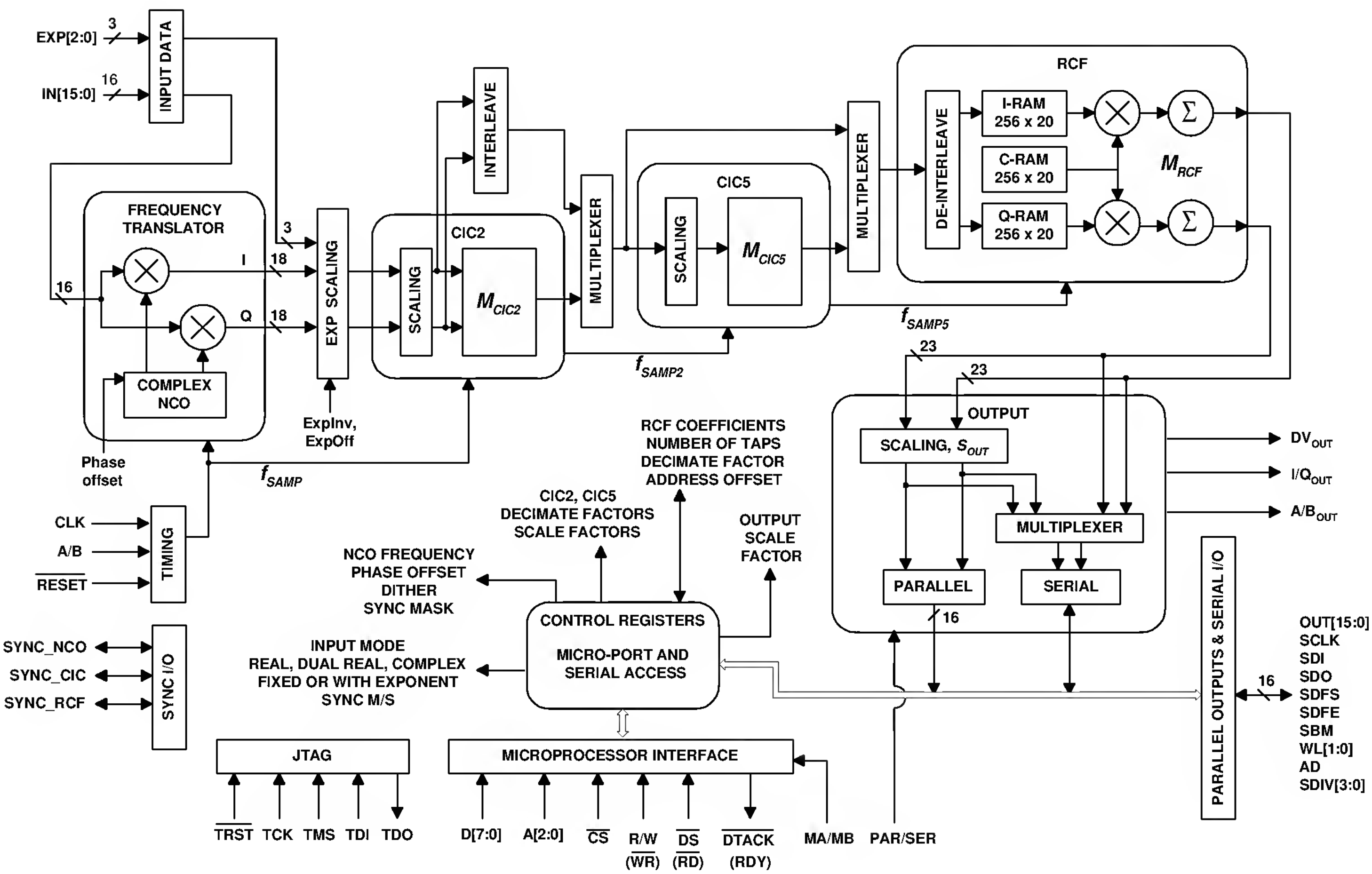
ARCHITECTURE

As shown in Figure 1, the AD6620 has four main signal processing stages: a Frequency Translator, two Cascaded Integrator Comb FIR Filters (CIC2, CIC5), and a RAM Coefficient FIR Filter (RCF). Multiple modes are supported for clocking data into and out of the chip. Programming and control is accomplished via serial and microprocessor interfaces.

Input data to the chip may be real or complex. If the input data is real, it may be clocked in as a single channel or interleaved with a second channel. The two-channel input mode, called Dual Channel Real, is typically used in diversity receiver applications. Input data is clocked in 16-bit parallel words, IN[15:0]. This word may be combined with exponent input bits EXP[2:0] when the AD6620 is being driven by floating-point or gain-ranging analog-to-digital converters such as the AD6600.

Frequency translation is accomplished with a 32-bit complex Numerically Controlled Oscillator (NCO). Real data entering this stage is separated into in-phase (I) and quadrature (Q) components. This stage translates the input signal from a digital intermediate frequency (IF) to baseband. Phase and amplitude dither may be enabled on-chip to improve spurious performance of the NCO. A phase offset word is available to create a known phase relationship between multiple AD6620's.

Following frequency translation is a fixed coefficient, high speed decimating filter that reduces the sample rate by a programmable ratio between 1 and 16 (Note: Decimation of 1 in CIC2 requires 2X or greater clock into AD6620). This is a second order, cascaded integrator comb FIR filter shown as CIC2 in Figure 1. The data rate into this stage equals the input data rate, f_{samp}. The data rate out of CIC2, f_{samp2}, is determined by the decimation factor, M_{CIC2}.



Following CIC2 is a second fixed-coefficient, decimating filter. This filter, CIC5, further reduces the sample rate by a programmable ratio from 1 to 32. The data rate out of CIC5, f_{samp5}, is determined by the decimation factor, M_{CIC5}.

Each CIC stage is a FIR filter whose response is defined by the decimation rate. The purpose of these filters is to reduce the data rate of the incoming signal so that the final filter stage, a FIR RAM coefficient sum-of-products filter (RCF), can calculate more taps per output. As shown in Figure 1, on-chip multiplexers allow both CIC filters to be bypassed if desired.

The fourth stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 32. The RAM Coefficient FIR Filter (RCF in Figure 1) can handle a maximum of 256 taps.

The overall filter response for the AD6620 is the composite of all three cascaded decimating filters: CIC2, CIC5, and RCF. Each successive filter stage is capable of narrower transition bandwidths but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage will minimize overall power consumption. Data comes out via a parallel port or a serial interface.

Figure 2 illustrates the basic function of the AD6620: to select and filter a single channel from a wide input spectrum. The frequency translator “tunes” the desired carrier to baseband. CIC2 and CIC5 have fixed order responses; the RCF filter provides the sharp transitions. More detail is provided in later sections of the datasheet.

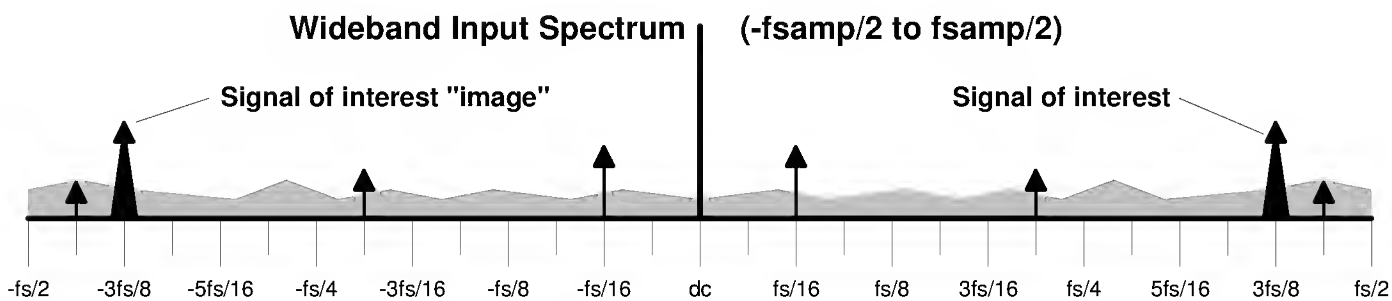


Figure 2a. Wideband Input Spectrum (e.g. 30MHz from Highspeed ADC)

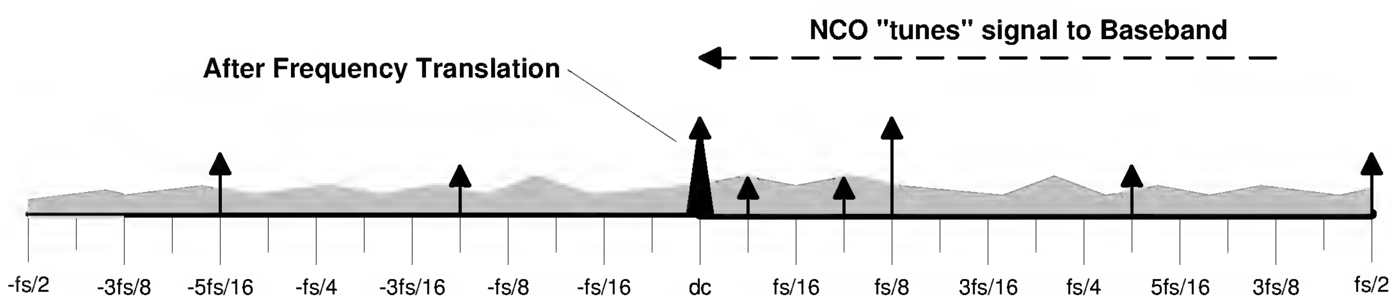


Figure 2b. Frequency Translation (e.g. single 1MHz channel tuned to basband)

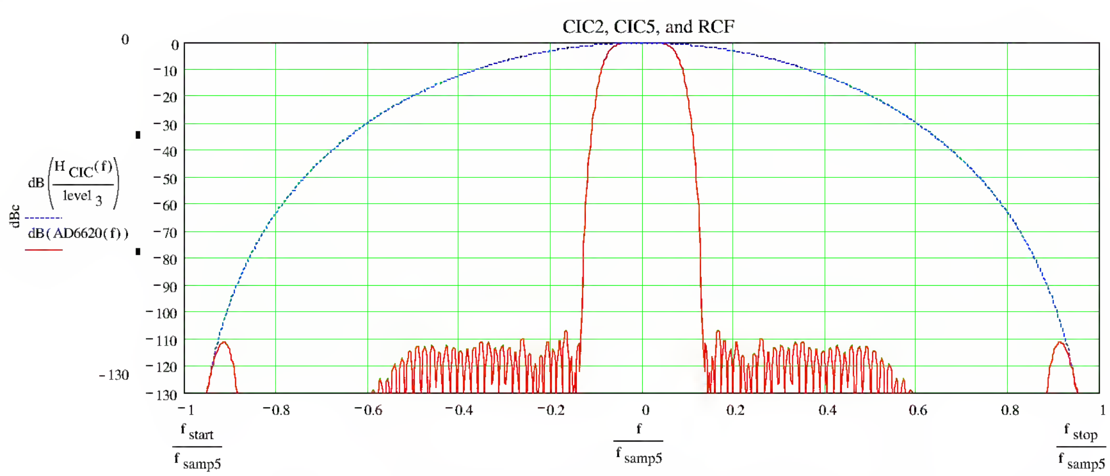


Figure 2c. Baseband signal is decimated and filtered by CIC2, CIC5, RCF

PACKAGE OUTLINE

80-Terminal Plastic Quad Flatpack (PQFP)